WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns;

a plurality of write word lines arranged individually for each of said plurality of memory cells, each of said plurality of memory cells including a data storage portion holding data, a data write portion writing data into said data storage portion, and a data read portion having a read bit line for reading data from said data storage portion, said data storage portion having first and second inverter circuits connected in common to a power supply line arranged corresponding to respective columns of said plurality of memory cells; and

a power supply line level control circuit controlling a potential level of said power supply line to a power supply potential or to a prescribed potential level lower than the power supply potential in response to a level control signal set for each column.

2. The semiconductor memory device according to claim 1, wherein

said power supply line level control circuit controls the potential level of said power supply line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said power supply line to the power supply potential with respect to a selected column and to said prescribed potential level with respect to a non-selected column respectively during a reading operation.

3. The semiconductor memory device according to claim 1, further comprising a ground line level control circuit controlling a potential level of a ground line to a ground potential, the power supply potential or floating for each column in response to said level control signal, wherein

said data read portion includes a transistor having a gate connected to a read terminal of said data storage portion, and having a source connected to the ground line of which potential level can be controlled.

4. The semiconductor memory device according to claim 3, wherein said ground line level control circuit controls the potential level of said ground line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said ground line to the ground potential with respect to a selected column and to the power supply potential or floating with respect to a non-selected column respectively during a reading operation.

5. The semiconductor memory device according to claim 1, wherein said power supply line level control circuit includes a plurality of power supply line level switching circuits provided for each column and switching the potential level of said power supply line to the power supply potential, a plurality of prescribed potential levels lower than the power supply potential, or floating for each column, in response to at least one of a retention test control signal, a redundancy replacement control signal, a plurality of retention potential setting signals, and said level control signal.

6. The semiconductor memory device according to claim 5, wherein said power supply line level switching circuit switches the potential level of said power supply line to the power supply potential during access and retention test, switches the potential level of said power supply line to the power supply potential or said plurality of prescribed potential levels during non-access, and switches the potential level of said power supply line to floating during redundancy replacement.

7. The semiconductor memory device according to claim 5, further comprising a setting signal control circuit controlling a logic level of said plurality of retention potential setting signals in synchronization with a clock signal in accordance with magnitude of the power supply potential.

8. The semiconductor memory device according to claim 7, wherein said setting signal control circuit includes
a first potential level adjustment circuit outputting a first power

supply potential shift signal having the potential level lower than the power supply potential by a prescribed value, in synchronization with said clock signal,

a second potential level adjustment circuit outputting a second power supply potential shift signal having the potential level lower than said first potential level by a prescribed value, in synchronization with said clock signal,

a first latch circuit outputting a first select control signal in accordance with a result obtained by comparison with an input threshold voltage, upon receiving said first power supply potential shift signal, and

a second latch circuit outputting a second select control signal in accordance with a result obtained by comparison with said input threshold voltage, upon receiving said second power supply potential shift signal, and

said setting signal control circuit controls the logic level of said plurality of retention potential setting signals in accordance with a combination of said first and second select control signals.

9. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns;

a plurality of write word lines arranged individually for each of said plurality of memory cells, each of said plurality of memory cells including a data storage portion holding data, a data write portion writing data into said data storage portion, and a data read portion having a read bit line for reading data from said data storage portion, said data storage portion having a first inverter circuit connected to a first power supply line arranged corresponding to respective columns of said plurality of memory cells and a second inverter circuit connected to a second power supply line arranged corresponding to respective columns of said plurality of memory cells; and

a power supply line level control circuit controlling a potential level of said second power supply line to a power supply potential or to a prescribed potential level lower than the power supply potential for each column in response to a level control signal set for each column.

10. The semiconductor memory device according to claim 9, wherein

said power supply line level control circuit controls the potential level of said second power supply line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said second power supply line to the power supply potential with respect to a selected column and to said prescribed potential level with respect to a non-selected column respectively during a reading operation.

11. The semiconductor memory device according to claim 9, wherein

said power supply line level control circuit includes a plurality of power supply line level switching circuits provided for each column and switching the potential level of said power supply line to the power supply potential, a plurality of prescribed potential levels lower than the power supply potential, or floating for each column, in response to at least one of a retention test control signal, a redundancy replacement control signal, a plurality of retention potential setting signals, and said level control signal.

12. The semiconductor memory device according to claim 11, wherein

said power supply line level switching circuit switches the potential level of said power supply line to the power supply potential during access and retention test, switches the potential level of said power supply line to the power supply potential or said plurality of prescribed potential levels during non-access, and switches the potential level of said power supply line to floating during redundancy replacement.

13. The semiconductor memory device according to claim 11, further comprising a setting signal control circuit controlling a logic level of said plurality of retention potential setting signals in synchronization with a clock signal in accordance with magnitude of the power supply potential.

14. The semiconductor memory device according to claim 13, wherein

said setting signal control circuit includes

a first potential level adjustment circuit outputting a first power supply potential shift signal having the potential level lower than the power supply potential by a prescribed value, in synchronization with said clock signal,

a second potential level adjustment circuit outputting a second power supply potential shift signal having the potential level lower than said first potential level by a prescribed value, in synchronization with said clock signal,

a first latch circuit outputting a first select control signal in accordance with a result obtained by comparison with an input threshold voltage, upon receiving said first power supply potential shift signal, and

a second latch circuit outputting a second select control signal in accordance with a result obtained by comparison with said input threshold voltage, upon receiving said second power supply potential shift signal, and

said setting signal control circuit controls the logic level of said plurality of retention potential setting signals in accordance with a combination of said first and second select control signals.

15. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns; and

a plurality of write word lines arranged individually for each of said plurality of memory cells; wherein

each of said plurality of memory cells includes

a data storage portion holding data,

a data write portion writing data into said data storage portion, and

a data read portion having a read bit line for reading data from said data storage portion, and

said data storage portion has

a first inverter circuit operating at a power supply potential or a

prescribed potential level lower than the power supply potential in response to a level control signal set for each column, and

a second inverter circuit operating at said prescribed potential level.

16. The semiconductor memory device according to claim 15,

said first inverter circuit includes

a first transistor connected between a first node and a first storage node,

a second transistor connected between the first storage node and a ground node, and

a third transistor connected between a power supply node and the first node and receiving said level control signal at a control terminal, and

said second inverter circuit includes

a fourth transistor connected between the first node and a second storage node,

a fifth transistor connected between the second storage node and the ground node, and

a sixth transistor diode-connected between the power supply node and the first node.

17. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns; and

a plurality of write word lines arranged individually for each of said plurality of memory cells; wherein

each of said plurality of memory cells includes

a data storage portion holding data,

a data write portion writing data into said data storage portion, and

a data read portion having a read bit line for reading data from said data storage portion, and

said data storage portion has

a first inverter circuit operating at a power supply potential or a prescribed potential level lower than the power supply potential in response

to a level control signal set for each column and a second level control signal set for each row, and

a second inverter circuit operating at said prescribed potential level.

18. The semiconductor memory device according to claim 17, wherein

said first inverter circuit includes

a first transistor connected between a first node and a first storage node,

a second transistor connected between the first storage node and a ground node,

a third transistor connected between a second node and the first node and receiving said level control signal at a control terminal, and

a seventh transistor connected between a power supply node and the second node and receiving said second level control signal at a control terminal, and

said second inverter circuit includes

a fourth transistor connected between the first node and a second storage node,

a fifth transistor connected between the second storage node and the ground node, and

a sixth transistor diode-connected between the power supply node and the first node.

19. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns;

a plurality of write word lines arranged individually for each of said plurality of memory cells, each of said plurality of memory cells including a data storage portion holding data, a data write portion writing data into said data storage portion, and a data read portion having a read bit line for reading data from said data storage portion, and said data storage portion having first and second inverter circuits connected in common to a ground line arranged corresponding to respective columns of said plurality of

memory cells; and

a ground line level control circuit controlling a potential level of said ground line to a ground potential or to a prescribed potential level higher than the ground potential in response to a level control signal set for each column.

20. The semiconductor memory device according to claim 19,

said ground line level control circuit controls the potential level of said ground line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said ground line to the ground potential with respect to a selected column, and to said prescribed potential level with respect to a non-selected column respectively during a reading operation.

21. The semiconductor memory device according to claim 19, further comprising a second ground line level control circuit controlling the potential level of a ground line to the ground potential, a power supply potential or floating for each column in response to said level control signal, wherein

said data read portion includes a transistor having a gate connected to a read terminal of said data storage portion, and having a source connected to the ground line of which potential level can be controlled.

22. The semiconductor memory device according to claim 21, wherein

said second ground line level control circuit controls the potential level of said ground line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said ground line to the ground potential with respect to a selected column, and to the power supply potential or floating with respect to a non-selected column respectively during a reading operation.

23. The semiconductor memory device according to claim 19,

wherein

said ground line level control circuit includes a plurality of ground line level switching circuits provided for each column and switching the potential level of said ground line to the ground potential, a plurality of prescribed potential levels higher than the ground potential, or floating for each column, in response to at least one of a retention test control signal, a redundancy replacement control signal, a plurality of retention potential setting signals, and said level control signal.

24. The semiconductor memory device according to claim 23,

said ground line level switching circuit switches the potential level of said ground line to the ground potential during access and retention test, switches the potential level of said ground line to the ground potential or said plurality of prescribed potential levels during non-access, and switches the potential level of said ground line to floating during redundancy replacement.

25. The semiconductor memory device according to claim 23, further comprising a setting signal control circuit controlling a logic level of said plurality of retention potential setting signals in synchronization with a clock signal in accordance with magnitude of the power supply potential.

26. The semiconductor memory device according to claim 25, wherein

said setting signal control circuit includes

a first potential level adjustment circuit outputting a first power supply potential shift signal having the potential level lower than the power supply potential by a prescribed value, in synchronization with said clock signal,

a second potential level adjustment circuit outputting a second power supply potential shift signal having the potential level lower than said first potential level by a prescribed value, in synchronization with said clock signal,

a first latch circuit outputting a first select control signal in accordance with a result obtained by comparison with an input threshold voltage, upon receiving said first power supply potential shift signal, and

a second latch circuit outputting a second select control signal in accordance with a result obtained by comparison with said input threshold voltage, upon receiving said second power supply potential shift signal, and

said setting signal control circuit controls the logic level of said plurality of retention potential setting signals in accordance with a combination of said first and second select control signals.

27. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns;

a plurality of word lines arranged for each row of said plurality of memory cells;

a plurality of bit line pairs arranged for each column of said plurality of memory cells, each of said plurality of memory cells including a data storage portion holding data, and a data write/read portion performing write/read of data to/from said data storage portion, and said data storage portion having first and second inverter circuits connected in common to a power supply line arranged corresponding to respective columns of said plurality of memory cells; and

a power supply line level control circuit controlling a potential level of said power supply line to a power supply potential or to a prescribed potential level lower than the power supply potential for each column in response to a level control signal set for each column.

28. The semiconductor memory device according to claim 27,

said power supply line level control circuit controls the potential level of said power supply line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said power supply line to the power supply potential with respect to a selected column and to said prescribed potential level with respect to a non-selected column respectively during a reading operation.

29. The semiconductor memory device according to claim 27, wherein

said power supply line level control circuit includes a plurality of power supply line level switching circuits provided for each column and switching the potential level of said power supply line to the power supply potential, a plurality of prescribed potential levels lower than the power supply potential, or floating for each column, in response to at least one of a retention test control signal, a redundancy replacement control signal, a plurality of retention potential setting signals, and said level control signal.

30. The semiconductor memory device according to claim 29, wherein

said power supply line level switching circuit switches the potential level of said power supply line to the power supply potential during access and retention test, switches the potential level of said power supply line to the power supply potential or said plurality of prescribed potential levels during non-access, and switches the potential level of said power supply line to floating during redundancy replacement.

31. The semiconductor memory device according to claim 30, further comprising a setting signal control circuit controlling a logic level of said plurality of retention potential setting signals in synchronization with a clock signal in accordance with magnitude of the power supply potential.

32. The semiconductor memory device, according to claim 31, wherein

said setting signal control circuit includes

a first potential level adjustment circuit outputting a first power supply potential shift signal having the potential level lower than the power supply potential by a prescribed value, in synchronization with said clock signal,

a second potential level adjustment circuit outputting a second power supply potential shift signal having the potential level lower than

said first potential level by a prescribed value, in synchronization with said clock signal,

a first latch circuit outputting a first select control signal in accordance with a result obtained by comparison with an input threshold voltage, upon receiving said first power supply potential shift signal, and

a second latch circuit outputting a second select control signal in accordance with a result obtained by comparison with said input threshold voltage, upon receiving said second power supply potential shift signal, and

said setting signal control circuit controls the logic level of said plurality of retention potential setting signals in accordance with a combination of said first and second select control signals.

33. A semiconductor memory device, comprising:

a plurality of memory cells arranged in matrix of rows and columns;

a plurality of word lines arranged for each row of said plurality of memory cells;

a plurality of bit line pairs arranged for each column of said plurality of memory cells, each of said plurality of memory cells including a data storage portion holding data, and a data write/read portion performing write/read of data to/from said data storage portion, and said data storage portion having first and second inverter circuits connected in common to a ground line arranged corresponding to respective columns of said plurality of memory cells; and

a ground line level control circuit controlling a potential level of said ground line to a ground potential or to a prescribed potential level higher than the ground potential for each column in response to a level control signal set for each column.

34. The semiconductor memory device according to claim 33, wherein

said ground line level control circuit controls the potential level of said ground line to said prescribed potential level for each column during a non-reading operation, and controls the potential level of said ground line to

the ground potential with respect to a selected column and to said prescribed potential level with respect to a non-selected column respectively during a reading operation.

35. The semiconductor memory device according to claim 33, wherein

said ground line level control circuit includes a plurality of ground line level switching circuits provided for each column and switching the potential level of said ground line to the ground potential, a plurality of prescribed potential levels higher than the ground potential, or floating for each column, in response to at least one of a retention test control signal, a redundancy replacement control signal, a plurality of retention potential setting signals, and said level control signal.

36. The semiconductor memory device according to claim 35, wherein

said ground line level switching circuit switches the potential level of said ground line to the ground potential during access and retention test, switches the potential level of said ground line to the ground potential or said plurality of prescribed potential levels during non-access, and switches the potential level of said ground line to floating during redundancy replacement.

37. The semiconductor memory device according to claim 35, further comprising a setting signal control circuit controlling a logic level of said plurality of retention potential setting signals in synchronization with a clock signal in accordance with magnitude of the power supply potential.

38. The semiconductor memory device according to claim 37, wherein

said setting signal control circuit includes

a first potential level adjustment circuit outputting a first power supply potential shift signal having the potential level lower than the power

supply potential by a prescribed value, in synchronization with said clock signal,

a second potential level adjustment circuit outputting a second power supply potential shift signal having the potential level lower than said first potential level by a prescribed value, in synchronization with said clock signal,

a first latch circuit outputting a first select control signal in accordance with a result obtained by comparison with an input threshold voltage, upon receiving said first power supply potential shift signal, and

a second latch circuit outputting a second select control signal in accordance with a result obtained by comparison with said input threshold voltage, upon receiving said second power supply potential shift signal, and

said setting signal control circuit controls the logic level of said plurality of retention potential setting signals in accordance with a combination of said first and second select control signals.